Qualitative Modelling of Linear Networks in ECAD Applications

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Abstract

There is a real need for qualitative circuit analysis tools in the ECAD application area. Recent simulators based on finite many valued resistance and current models (switch-level models) have been shown to have serious limitations. Through independent parallel research the QR community has produced qualitative electrical models and simulators that have been successfully used in software tools for specific engineering tasks. Many of these systems are based on steady-state models using three valued resistance networks.

This paper examines the relationship between qualitative and more conventional electrical circuit modelling and explores the characteristics of certain qualitative formulations with a view to satisfying the needs of future intermediate level models. An existing three valued resistance model is analysed and then extended to deal with additional cases. The problems associated with bridge circuits may pose a major barrier to future progress and this is examined in detail and some solutions are described.

The Importance of Qualitative Concepts in ECAD

There has been a long standing interest in the ECAD community to find an intermediate modelling level between the gate-level simulators and other analysis tools used in digital logic and the electrical analogue simulators that work at the transistor level. Circuit analysis often involves predictions of *both* logical/state information and details of electrical parameters and ideally this should be performed in an integrated and coherent environment. While it is possible to model a complete circuit on an analogue simulator this does not capture the distinct qualitative states that characterise important abstractions valued by engineers. Even more important is the problem of maintaining close affinities between the properties of the model and the preferred notations and concepts used by human engineers. This is very difficult to achieve with the voluminous numeric output generated by conventional simulators. This problem is confirmed by reports from ECAD experts who have access to considerable data on engineers' experience, e.g.

> "Graphical interfaces can present simulation data in more convenient forms, but they do not interpret their meaning nor do they reduce the number of simulations required in order to gain a feel about some circuit performance. It has thus become clear that numerical descriptions of circuit behaviour do not convey understanding about the operation of a circuit. In fact, the use of such numerical-only systems can impose a barrier to the development of insight." (Makris and Toumazou 1992)

An early attack on this problem produced the "Switch-Level Models" developed by Hayes and others in the last decade. This work aimed to build circuit models intermediate between gate-level simulators and analogue electrical models (Hayes 1986, 1987). The variables, known as "magnitude classes", had value pairs consisting of a four-valued voltage level and an n-valued signal strength (or current) value.

After a great deal of development in the 1980s, Hayes final paper in 1992 described the severe accuracy limitations that prevented any further development of switch-level models (Cerny et al. 1992). Thorough analysis showed that the accuracy of the higher order models was no better than those with only two or three levels:

> "A major conclusion from our work is that switch-level simulators which use many signal strength classes may have no better accuracy than simulators in which only two or three strengths are used to distinguish very large differences in resistance values." (Cerny et al. 1992)

Hayes has recently stated that there is now a renewed and pressing need to overcome these problems and provide an intermediate-valued model for use at the important interface between dense numerical detail and the sparseness of extreme qualitative representations.

The Significance of QR Circuit Models

Without any apparent knowledge of the switch-level model experiments, the QR community has independently developed qualitative electrical models and investigated their application to significant problems in design and analysis. There are various approaches to

modelling electrical circuits using qualitative abstractions of electrical properties, a classic study being (de Kleer 1984), but we are concerned with steady-state rather than dynamic models. Quiescent current resistance models have been examined recently by several authors. (Struss et al. 1996) used a qualitative resistance model in applications in diagnosis and FMEA and (Mauss and Neumann 1996) have investigated the use of the series/parallel/star/delta replacement rules to convert any resistive mesh into a single equivalent resistor. Flores and Farley have applied similar series/parallel decompositions to analyse alternating current circuits (Flores and Farley 1996). Most of these methods have in common the idea of a three valued resistive mesh abstraction which was first explored by (Lee and Ormsby 1992).

The motivation for the QR work has been to address various significant tasks like diagnosis, design and analysis. Software tools are now being developed for such applications and embody qualitative models in contrast to the numerical equation solvers used in most electrical simulation packages. In this paper we mainly draw on our own work on qualitative circuit theory, known as CIRQ (Lee and Ormsby 1993), which addresses the requirements of the analysis task of FMEA (Failure Mode Effects Analysis). This theory underpins one of the most advanced commercial systems in regular use for electrical FMEA in the automobile industry (Price et al. 1992, 1995).

The switch-level modelling work was built from many-valued logic and hence had a symbolic rather than a numeric grounding. It was different in its assumptions, approach and target circuits from QR work but in many ways had very similar aims. The voltage variable was 4-valued and therefore was essentially qualitative. Voltage values were taken from $[+,-,0,\mathrm{U}]$ which represented the two supply potentials, an intermediate potential, and an open circuit, respectively. In CIRQ the symbol set for voltage is $[0,+,\sim,\emptyset]$ where 0 and + are the supply terminals, $\emptyset$ is a special symbol implying a "floating" or disconnected node and $\sim$ indicates a voltage between the supply potentials[1]. It is clear that the semantics of these are practically identical and the equivalence between these independent developments is most striking.

In most of the recent steady state resistance models qualitative resistance values are three valued and of the form $[0,+,\infty]$ representing a conductor, an energy absorbing load and an insulator respectively. Switch-level models had a finite set of resistance values which also included 0 and ∞ but gave scope for finer resolution by including $n-1$ intermediate levels, where $R_{i+1} > R_i$. With a fixed voltage, Ohm's law gives an equivalent range of current levels corresponding in number to the resistances. The combination of the voltage and $n+1$ current values gives $3n+1$ symbols that could be assigned to circuit elements. In the simulators described, current usually had 3 or 4 levels and so the number of discrete labels was 10 or 13.

[1]Previous work has also used $[-,+,\sim,0]$ as an alternate symbol set.

The CIRQ Algorithm

We now briefly describe the main features of the CIRQ approach. Circuits are constructed from library components which are specified as resistive meshes between defined terminals. This allows the whole circuit to be modelled as a graph E(T, R) containing T nodes and R weighted edges corresponding to resistive elements. The edges are assigned qualitative resistance values from the set $[0,n,\infty]$ where *any positive integer*, $n \in \mathcal{N}$, signifies a load resistance. Normally we restrict all resistive loads to unity. As described above, qualitative voltage values are $[0,+,\sim,\emptyset]$ and qualitative current is two-valued $[0,+]$ corresponding to absence or presence of electrical activity in an edge.

The physics of series and parallel circuit reduction require the numeric summation of their resistances or their conductances respectively. The standard qualitative version of this uses Max and Min as the series and parallel reduction rules, given the ordinal relationship $0 < n < \infty$. For reasons that will become clear, we modify this slightly and use Sum, rather than Max for the series reduction rule. As we are using positive integers this has no effect whatsoever on the results as any positive integer produced from Sum remains distinct from 0 and ∞. The Sum function adds the values of load resistances on serial paths and we define the result of this as the **path resistance**, $PR(s,t)$, between any two nodes s and t. When parallel branches are combined the Min function ensures that shortest paths are returned and so the single equivalent resistance value found by applying series/parallel reduction transforms to a network between terminals s and t is the same as the value of the shortest path between s and t using the resistive edge weights.

The labelling algorithm is a shortest distance algorithm that begins from one power terminal and assigns the minimum path resistance value to each node's forward label, then the reverse labels are assigned by a repeat process starting from the other terminal. These variables are stored in each node as *forward* and *reverse* path resistances, known as f/r. All f/r values are initialised to ∞/∞ because any sub-graphs disconnected from the supply terminals are not traversed and so return appropriate values. Figure 1 illustrates this process. As a new edge from v to w is explored its resistance, R, is added to the parent node value using the series rule and this result is then combined with any existing value representing a parallel path using the parallel rule. In figure 1(a) all edges have resistance value unity and the node u has produced labels for its successors w and v. Node v is currently being processed and so $4+1$ is to be combined with the existing value of 4 at node w. Thus a final result of 4 is produced.

Clearly, any quantitative form of this traversal process would fail because combining the branches of a

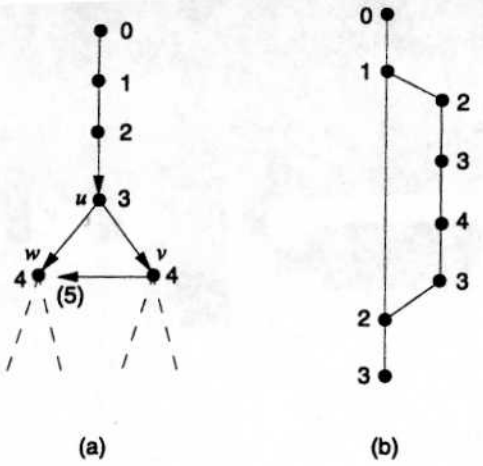

Figure 1: The CIRQ labelling process

parallel circuit would affect the previously calculated values on any series sections. It might be expected that this problem would also occur in qualitative cases where one series branch has a much higher value than another. However, this does not happen because the labelling process always explores the lowest valued nodes first. Figure 1(b) shows how a long series branch is labelled. This topology causes the algorithm to enter the right-hand branch from both ends and thus each node is assigned its correct minimum path length from the start node.

When all the nodes are labelled their qualitative voltages are assigned according to their f/r values as shown in table 1.

Node value		Interpretation	
f	r	Condition	Voltage
0	0	Short across supply	$\sim$
0	+	Active path through node	+
0	∞	Dead node	+
+	0	Active path through node	0
+	+	Active path through node	$\sim$
+	∞	Dead node	+
∞	0	Dead node	0
∞	+	Dead node	0
∞	∞	Dead sub-graph	$\emptyset$

Table 1: Mapping f/r values into voltage

During the traversal all electrically identical nodes (i.e. connected by a path of zero resistance) are grouped into *supernodes*. The supernode concept facilitates a block detection algorithm that assigns zero current to any dead or shorted branches. All 2-connected blocks are identified then all edges in the block containing the power terminals are labelled active and all edges in other blocks are labelled inactive. Figure 2 shows the supernode structure of an example circuit with the active parts marked.

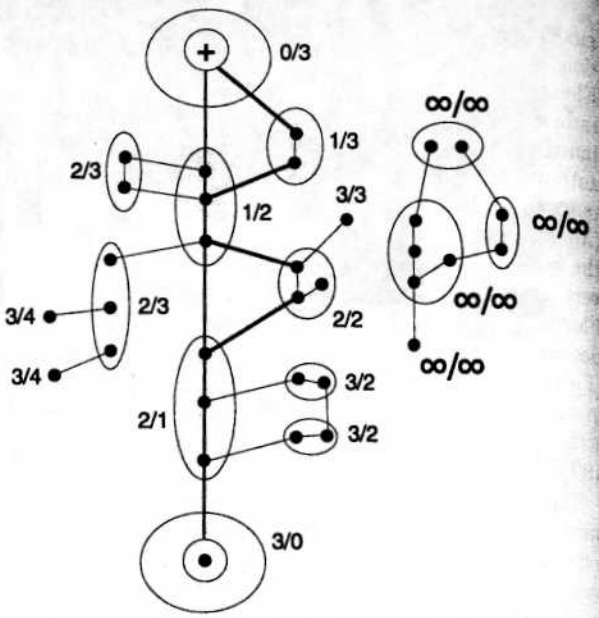

Figure 2: Supernodes in a circuit

Why does CIRQ work?

Circuits that can be reduced to a single equivalent resistance by repeated application of only series/parallel reduction rules are called SP reducible. However, many circuits have a topology that is not SP reducible, see examples in figure 3.

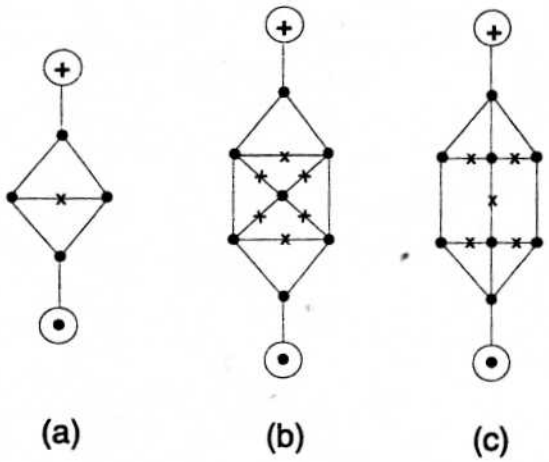

Figure 3: Examples of non SP reducible circuits

For numerical solution, any non SP reducible circuits require the application of additional transform rules such as the star/delta conversion equations. Other authors (Mauss and Neumann 1996) have stated that algorithms like CIRQ can not cope with non SP reducible networks but this is incorrect. It is perhaps surprising that using only series/parallel reduction rules CIRQ can analyse *any* topology of circuit, including non SP re-

ducible networks. This raises some important issues which we now examine.

We defined the path resistance $PR(s,t)$ between two nodes, s and t, as the value of a single equivalent resistance found by applying reduction transforms to the sub-network that comprises all paths from s to t. Our choice of Sum and Min for the reduction functions combines the requirements of 3-valued resistance transforms with shortest path criteria. The reduction operations on 3-valued series and parallel circuits are correctly performed for qualitative evaluation of SP reducible circuits while also being directly equivalent to the shortest path in terms of the resistive edge weights. This equivalence allows us to employ a traversal algorithm to label the nodes. From the node resistance labels the voltages are determined and then loops and dead branches are removed by graph-theoretic methods. For SP reducible networks it is clear that CIRQ is complete and in addition is able to produce flow directional labels. Edge current flow direction are related to the node resistance values and so flow direction can be determined as follows. Let a simple series path exist between end nodes u and v and define

$$F(u) = \frac{f(u)}{f(u) + r(u)}$$

then

$$\text{direction of flow is:} = \begin{cases} \text{from } u \text{ to } v & \text{if } F(u) < F(v) \\ \text{from } v \text{ to } u & \text{if } F(u) > F(v) \\ \text{ambiguous} & \text{if } F(u) = F(v) \end{cases}$$

This can be used to assign labels for SP reducible networks, see (Lee and Ormsby 1993) for examples of previous path following algorithms.

We now need to consider the non SP reducible case. The difference between SP reducible and irreducible circuits is the existence of bridging edges. Non SP reducible circuits have two types of edges: main flow edges that can be labelled for current magnitude and direction just as for SP reducible circuits, and "bridges" that connect different flow paths and in which both flow direction and magnitude are ambiguous. The circuits in figure 3 are all non SP reducible examples where the current magnitude and direction can be labelled in the non-bridge (unmarked) edges but are ambiguous in the bridge (marked) edges. If bridges have identical voltage potential at each end then they have zero current flow and are said to be balanced. To illustrate the subtleties of bridge configurations, figure 4 shows the three possible assignments for the central bridge in the circuit of figure 3(c). It is interesting that a configuration exists where reverse flow occurs in the central bridge.

In all cases except for bridges CIRQ correctly labels both current directions and current magnitude (2-valued). For any bridges CIRQ always labels current as active and direction as either ambiguous (correct) or in the direction of majority flow paths (strictly incorrect). Figure 5 shows a case where the labelling scheme has given plausible directions to the central bridges but

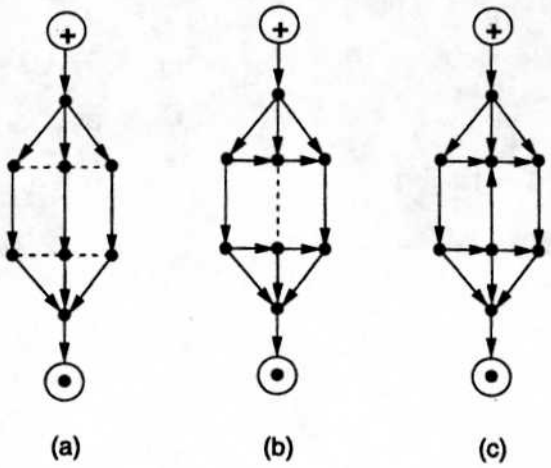

Figure 4: The 3 flow cases for the central edge in figure 3(c)

these are essentially ambiguous as reverse flow is possible in some unusual configurations.

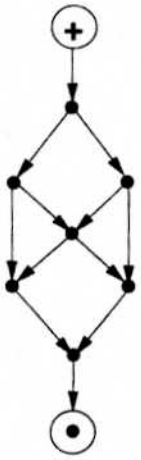

Figure 5: Bridging edges erroneously labelled for direction

These assignments by CIRQ are acceptable for the FMEA application where bridges are treated separately and flow direction is of secondary importance. In general circuit analysis, however, the bridge topology is a recurring difficulty. This is because the direction of current flow depends upon the *exact quantitative values* of resistance in the associated bridge components. This is a problem for all qualitative resistance representations as it is impossible to deduce the state of a bridge element without quantitative values. Consequently the best any quantitative analysis of bridge circuits can return is an "ambiguous" direction label. This is what is done in the methods that use series/parallel/star reduction rules (Mauss and Neumann 1996) and comparisons with CIRQ show that this produces results with identical qualitative meaning.

Limitations of Qualitative Resistance Models

For FMEA of the kind required for automotive circuit analysis, CIRQ type models are effective and efficient. Flow directions are not essential and balanced bridges are rare and can be isolated. CIRQ satisfies the specification of the FMEA task as open-circuit and power short-circuit faults have topological interpretations that are correctly reflected in the model. See (Lee 1999) for full details of this application.

However, for general use we must be aware of the effects of any limitations of qualitative circuit models. There are two questions that arise: how often do bridge circuits actually occur, and how might they be handled. For the first question we notice that in the general case of a resistive mesh with a single source and sink terminal, all edges are candidate bridge edges except those incident on the supply terminals. In the case of a planar mesh, the extreme edges bounding the network are also exempt. This means that in large highly connected meshes the majority of edges could be bridges. However, in practical applications such circuit topologies rarely occur. This is because most flow paths are concerned with a particular causal sequence through a chain of components running from one supply terminal to the other. Hence the topology of many realistic circuits has a branching structure with diverging and converging patterns. In addition, any bridging paths are usually clearly designed to provide flow in one direction only. Experience with many automotive circuits confirms that ambiguous or balanced bridges rarely occur in practice. In applications of CIRQ in automotive FMEA, (Snooke and Price 1997) report that 85% of the circuits encountered could be handled immediately with the remaining 15% requiring special treatment to deal with complex behaviour. These were handled either by building complex component models out of the primitive components, by constructing dependency links between active states and other components, or by applying approximating simplifications, which either reduce detail or even ignore some behaviour. There were no cases of balanced bridges and no other directional flow problems that could not be resolved.

The second question refers to the treatment of bridges in qualitative simulators. Given that inference of current from solely qualitative values is incomplete for any non SP system then at least we can detect whether a circuit is SP reducible or not. We have examined several methods for preprocessing circuits with bridge detection algorithms. We first notice that during the above directional labelling process, if the circuit is SP reducible then the label 'ambiguous' can not occur. Conversely, appearance of this label indicates a non SP reducible circuit. Unfortunately this criteria does not provide a complete test as some bridges may erroneously receive consistent directional assignments, an example of this was shown in figure 5.

We have designed a bridge detector using a graph-theoretic approach. An obvious algorithm for bridge detection is to enumerate all paths from source to sink and label each edge with the direction of traversal. Then any edges that have both directional labels are candidate bridges. However, such algorithms are closely related to Hamiltonian paths and have complexities in the region of O(n!). A more efficient algorithm is given by a breadth-first scan of the circuit, starting at the source terminal, and assigning "dewey decimal" type labels at each branch point. A label consists of a vector of indices, $x_1, x_2, x_i ... x_m$ where each index records the successor branch number at level i in the structure. When a new node is encountered the vector increases to add x_{m+1} which takes the value $1, 2, ...n$ for each successor branch. As the circuit diverges the labels expand, and then on convergence they either recombine (without conflict) or they clash, indicating a bridge.

```
procedure bridge-test (node, node-label, level)
put node at start of Queue
while not(empty(Queue)) do
      remove node w from Queue
      if w = null then return "no bridges"
          else for each node v ∈ adjacent(w) do
              if node-label(v) = null then new-label(v)
                 else update-label(v), if label- clash(v)
                              return "bridge-found"
              add v to end of Queue
      end-while
end bridge-test
```

Recombination involves the removal of the last vector element when all branches have been recovered and clashes occur when level j completes recombination before level i, where $j < i$. The algorithm is efficient in time but the node vector space demands considerable storage.

This bridge detector function gives a binary output for presence or otherwise of bridges, that is, it stops when the first bridge has been detected. Further development of the algorithm is required if the location of all bridges are to be found.

Solving circuits with orders-of-magnitude resistance

Another approach to the problem is to increase the number of resistance values to gain finer resolution. We found the orders-of-magnitude concept (Raiman 1991) offers a very promising solution. There is some evidence that five valued variables are preferred by engineers (Brna and Caiger 1992) and we introduce a qualitative resistance set $[0, lo, med, hi, \infty]$ which is ordered by $<<$. The semantics of lo, med and hi can be related to various ranges of numeric resistance values such as $10, 100, 1k$ ohms or $10, 1k, 100k$ ohms with orders of magnitude separation. Resistance is one of the physical variables with a vast range spanning many orders of magnitude and a promising possibility for applications is to separate by two orders of magnitude, e.g.

$100, 10k, 100M$ ohms. However, for simplicity and illustration we will use the scheme $[0, 1, 10, 100, \infty]$ in the CIRQ algorithm. The ordering relation maintains the shortest path criterion and so the three-valued semantics of $[0, n, \infty]$ ensure that the nodes will be labelled with voltage exactly as before. However the node path resistance values now produce much more information about flow directions. Previously the shortest path found was the route through the least number of resistive edges, now the result is the lowest valued resistance path. Figure 6 shows the result of CIRQ on the bridge circuit of figure 3(c). The high valued edges (marked *hi*) cause the main flow to follow the low resistance branches and the unusual reverse flow in the centre branch has been detected (q.v. figure 4(c)).

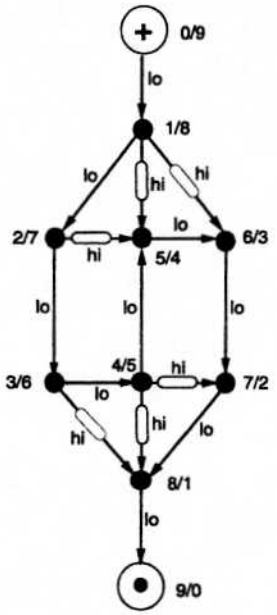

Figure 6: O-o-M resistance finds correct flow paths in non SP circuit

This is clearly seen in the node path resistance values which trace the longer main route which now involves 9 edges rather than the 5 of the shortest path.

Other circuits that can have bridge directions resolved by orders-of-magnitude resistance are shown in figure 7. Various constraints act between bridge configurations, for example in figure 7(a) the branches a and b can not both be zero and of the 9 possible circuit labellings (3 for each of a and b) only 5 are physically realisable. For figure 7(b) at least 2 of the 4 bridges must be non-zero and in figure 7(c) the central branch e has many configurations for downward flow but only 3 for zero and 2 for upward flow.

The Contribution from QR

Given that, in general, bridges cannot be resolved neither for current magnitude nor direction without precise quantitative values, we have explored the possibilities

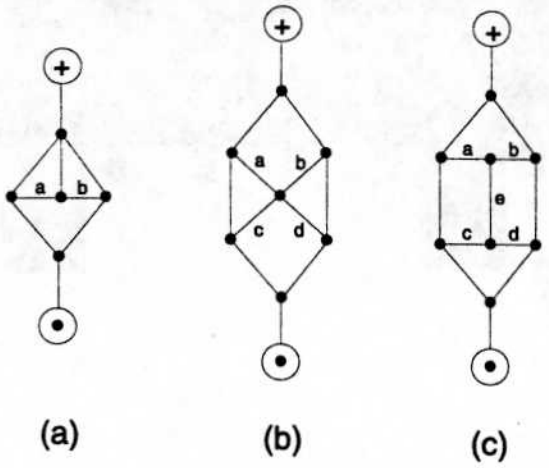

Figure 7: Non SP reducible circuits

of coping with this limitation in possible quantitative models for ECAD. There are three levels of difficulty: SP reducible circuits with no bridges, SP irreducible circuits with non-zero bridges, and SP irreducible circuits with balanced bridges.

We have designed methods for detecting bridges so that any SP reducible circuit can be immediately processed for complete results. We noticed that detecting bridges by ambiguity labels is rather like a semi-decidable problem and not reliable for non SP reducible cases.

For SP irreducible circuits with non-zero (unbalanced) bridges the orders-of-magnitude formulation is particularly promising. By using a larger set of resistance values separated by an orders-of-magnitude relation, directional flows can be decided that would otherwise remain ambiguous. The only remaining problem is the case of balanced bridges which will of necessity involve local resistance values from the same orders-of-magnitude band. As mentioned before, balance can not be determined by any qualitative method under such conditions. However, by increasing the number of resistance values we can resolve more and more cases of ambiguity. It will be interesting to consider the limits and trade-offs that occur from increasingly finer resolution.

The CIRQ process with m valued resistance, $R_{1..m}$ is correct for directional labels provided the number of resistances in a series path is always less than n where $R_{i+1} > 2nR_i$. Thus for a separation of 2 orders of magnitude we may allow up to 50 resistors in a series chain. This offers exciting possibilities for new models of circuits that give full directional routing of currents.

It is important to realise that we do not encounter the accuracy problems of the switch-level methods because we do not generate finer current values from the increased resistance set. Applying our fixed voltage and m resistance values to Ohm's law would produce m valued current but this is avoided and current remains two-

valued. Our approach can be seen as an overloading of the resistance value set for two different purposes: first as a 3-valued qualitative analysis to determine voltage and the existence (or not) of edge current, and secondly, as a tool for directional labelling in the active branches. As we do not calculate current magnitudes we do not need star/delta transform rules — series/parallel reductions in a shortest path traversal process is both sufficient and efficient for all topologies.

Qualitative models have strong intuitive appeal with engineers and often have more affinity with the real world problem than mathematical formulations. We hope the methods described here are a step towards an intermediate level that can be used in more conventional electrical circuit modelling environments.

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